CLAIMS

1. A stacked semiconductor device consisting of a first semiconductor device having outside electrode terminals on its lower surface, a second semiconductor device electrically connected with said first semiconductor device and secured on said first semiconductor device, characterized in that:

said first semiconductor device has:

a semiconductor substrate;

a multilayer wiring part including a plurality of circuit elements formed at a first main surface side of said semiconductor substrate and wiring connected with said circuit elements;

a first insulating layer for covering said multilayer wiring part;

a second insulating layer for covering a second main surface to become an opposite face against the first main surface of said semiconductor substrate;

a plurality of post electrodes formed on respective specified wiring of said multilayer wiring part to be exposed in a surface of said first insulating layer;

a plurality of through-type electrodes provided to pierce through said semiconductor substrate and said second insulating layer from specified depth of said multilayer wiring part, brought into contact to said semiconductor substrate through an insulating film and connected with specified wiring of said multilayer wiring part respectively; and

said outside electrode terminals connected to said through-type electrodes;

said second semiconductor device has:

a semiconductor substrate;

a multilayer wiring part including a plurality of circuit elements formed at a first main surface side of said semiconductor substrate and wiring connected with said circuit elements;

a first insulating layer for covering said multilayer wiring part;

a second insulating layer for covering a second main surface to become an opposite face against the first main surface of said semiconductor substrate;

at least post electrodes formed on respective specified wiring of said multilayer wiring part to be exposed in a surface of said first insulating layer or a plurality of through-type electrodes provided to pierce through said semiconductor substrate and said second insulating layer from specified depth of said multilayer wiring part, brought into contact to said semiconductor substrate through an insulating film and connected with specified wiring of said multilayer wiring part respectively, and

in said first semiconductor device, said post electrodes or said through-type electrodes come in a lower surface and said post electrodes or said through-type electrodes in the lower surface are provided with said outside electrode terminals;

said through-type electrodes or said post electrodes in the lower surface of said second semiconductor device are electrically connected with said post electrodes or said through-type electrodes in the upper surface of said first semiconductor device through joints.

2. The stacked semiconductor device according to claim 1 having a third semiconductor device stacked and secured between said first semiconductor device and said second semiconductor device over one to a plurality of steps, characterized in that:

said third semiconductor device has:

a semiconductor substrate;

multilayer wiring part including a plurality of circuit elements formed at a first main surface side of said semiconductor substrate and wiring connected with said circuit elements;

a first insulating layer for covering said multilayer wiring part;

a second insulating layer for covering a second main surface to become an opposite face against the first main surface of said semiconductor substrate;

a plurality of post electrodes formed on respective specified wiring of said multilayer wiring part to be exposed in a surface of said first insulating layer;

a plurality of through-type electrodes provided to pierce through said semiconductor substrate and said second insulating layer from specified depth of said multilayer wiring part, brought into contact to said semiconductor

substrate through an insulating film and connected with specified wiring of said multilayer wiring part respectively, and

the post electrodes or the through-type electrodes on the upper/lower surfaces of said third semiconductor device are electrically connected with the post electrodes or through-type electrodes of the semiconductor device at the upper stage side and the semiconductor device at the lower stage side through joints.

3. The stacked semiconductor device according to claim 1, characterized in that said semiconductor devices at the respective stages will become a single body and the respective semiconductor devices overlap each other in corresponding fashion in a same size.

4. The stacked semiconductor device according to claim 1, characterized in that a plurality of second semiconductor devices smaller than said first semiconductor device are disposed and secured in parallel on said first semiconductor device.

5. The stacked semiconductor device according to claim 1, characterized in that the respective through-type electrodes or the respective post electrodes on the upper surface of said first semiconductor device and the respective through-type electrodes or the respective post electrodes on the lower surface of said second semiconductor device are brought into correspondence and are electrically connected respectively through said joints.

6. The stacked semiconductor device according to claim 1, characterized in that said joints are not used for joining the respective through-type electrodes or the respective post electrodes on the upper surface of said first semiconductor device with the respective through-type electrodes or the respective post electrodes on the lower surface of said second semiconductor device but,

said post electrodes or said through-type electrodes engaged in said joining of said one semiconductor device protrude and those protruding portions are connected to said post electrodes or said through-type electrodes of the facing semiconductor device with metal joining.

7. The stacked semiconductor device according to claim 1, characterized in that said post electrodes are formed of a plating film, stud bump electrodes or a CVD film.

8. The stacked semiconductor device according to claim 1, characterized in that a metal plate having insulating holes is present between said first semiconductor device and said second semiconductor device, in the portion of said insulating holes, said through-type electrodes or said post electrodes on the upper surface of said first semiconductor device are electrically connected with said through-type electrodes or said post electrodes on the lower surface of said second semiconductor device through said joints in a state without contacting said metal plate, said through-type electrodes and said post electrodes of said first semiconductor device and said second semiconductor device to face said metal plate

are electrically connected with said metal plate through said joints.

9. The stacked semiconductor device according to claim 8, characterized in that said through-type electrodes or said post electrodes to be given power supply potential of said semiconductor device or ground potential are connected with said metal plate.

10. The stacked semiconductor device according to claim 1, characterized in that out of said first and second semiconductor devices, said semiconductor substrate of one semiconductor device is a silicon substrate and said semiconductor substrate of the other semiconductor device is a compound semiconductor substrate.

11. The stacked semiconductor device according to claim 1, characterized in that said through-type electrodes and said post electrodes are formed of copper, tungsten, titanium, nickel, aluminum or alloy thereof.

12. The stacked semiconductor device according to claim 1, characterized in that gap between said first semiconductor device and said second semiconductor device is filled with insulating resin.

13. The stacked semiconductor device according to claim 1, characterized in that said second semiconductor device has, likewise said first semiconductor device, a plurality of post electrodes exposed in a surface of said first insulating layer and a plurality of through-type electrodes exposed in a surface of said second insulating layer, and through-type electrodes

are formed at exposed ends of specified said post electrodes or said through-type electrodes located in the upper surface.

14. The stacked semiconductor device according to claim 1, characterized in that said post electrodes are larger than said through-type electrodes in diameter.

15. The stacked semiconductor device according to claim 1, characterized in that said circuit elements are active elements and passive elements.

16. The stacked semiconductor device according to claim 1, characterized in that said semiconductor substrates of said respective semiconductor devices have thickness of around 5 to 50 μm and said first insulating layer has thickness of around 20 to 100 μm.

17. A semiconductor device characterized by having:

a semiconductor substrate;

a multilayer wiring part including a plurality of circuit elements formed at a first main surface side of said semiconductor substrate and wiring connected with said circuit elements;

a first insulating layer for covering said multilayer wiring part;

a second insulating layer for covering a second main surface to become an opposite face against the first main surface of said semiconductor substrate;

a plurality of post electrodes formed on respective specified wiring of said multilayer wiring part to be exposed in a surface of said first insulating layer;

a plurality of through-type electrodes provided to pierce through said semiconductor substrate and said second insulating layer from specified depth of said multilayer wiring part, brought into contact to said semiconductor substrate through an insulating film and connected with specified wiring of said multilayer wiring part respectively.

18. The semiconductor device according to claim 17, characterized in that protruding electrodes are formed at exposed ends of specified said post electrodes and said through-type electrodes.

19. The semiconductor device according to claim 17, characterized in that said post electrodes are larger than said through-type electrodes in diameter.

20. The semiconductor device according to claim 17, characterized in that said post electrodes are formed by a plating film, stud bump electrodes or a CVD film.

21. The semiconductor device according to claim 17, characterized in that said through-type electrodes and said post electrodes are formed of copper, tungsten, titanium, nickel, aluminum or alloy thereof.

22. The semiconductor device according to claim 17, characterized in that said circuit elements are active elements and passive elements.

23. The semiconductor device according to claim 17, characterized in that said semiconductor substrates of said respective semiconductor devices have thickness of around 5 to 50 μm and said first insulating layer has thickness of around 20 to 100 μm.

24. A process for fabricating a stacked semiconductor device having a first semiconductor device having outside electrode terminals on its lower surface and a second semiconductor device stacked and secured on said first semiconductor device and said both semiconductor devices being brought into electrical connection, having:

(a) a step of aligning, disposing and forming a plurality of product forming parts inclusive of specified circuit elements on a first main surface of a semiconductor substrate;

(b) a step of forming a multilayer wiring part in said respective product forming parts by laminating and forming sequentially in a specified pattern wiring and insulating layers being connected electrically with said circuit elements;

(c) a step of forming, at the stage for forming said multilayer wiring part, a plurality of holes toward a second main surface to become an opposite face against said first main surface of said semiconductor substrate from specified depth of said multilayer wiring part having an insulating film on their surfaces and of forming filling electrodes to fill those holes with conductive substance and be electrically connected with specified wiring of said multilayer wiring part;

(d) a step of forming post electrodes on respectively specified wiring of said multilayer wiring part;

(e) a step of forming, on the first main surface of said semiconductor substrate, a first insulating layer to cover said post electrodes;

(f) a step of removing the surface of said first insulating layer by specified thickness to expose said post electrodes;

(g) a step of removing the second main surface of said semiconductor substrate from its surface by specified thickness to expose said filling electrodes to form through-type electrodes;

(h) a step of removing by etching the second main surface of said semiconductor substrate by specified thickness to cause said through-type electrodes to protrude by specified length;

(i) a step of forming a second insulating layer of specified thickness on the second main surface of said semiconductor substrate in a state of exposing forward ends of said through-type electrodes;

(j) a step of cutting the said semiconductor substrate inclusive of said first and second insulating layers in a lattice pattern to divide said respective product forming parts; and

(k) a step of forming protruding electrodes at specified exposed ends among said through-type electrodes and said post electrodes after said step (i) or after said step (j), wherein

through said step (a) to step (k), said first semiconductor device is formed;

through selection of said step (a) to step (k), said second semiconductor device having, at least, said through-type electrodes or said post electrodes is formed;

next, said first semiconductor device is disposed so that said through-type electrodes or said post electrodes

come to the lower surface to be regarded as said outside electrode terminals, and thereafter, said through-type electrodes or said post electrodes in the lower surface of said second semiconductor device and said through-type electrodes or said post electrodes in the upper surface of said first semiconductor device are brought into electrical connection with temporary melting treatment applied to said protruding electrodes to fabricate a stacked semiconductor device.

25. The process for fabricating a stacked semiconductor device according to claim 24, characterized in that said second semiconductor device having only said through-type electrodes is formed through:

a step of aligning, disposing and forming a plurality of product forming parts inclusive of specified circuit elements on a first main surface of said semiconductor substrate;

a step of forming a multilayer wiring part in said respective product forming parts by laminating and forming sequentially in a specified pattern wiring and insulating layers being connected electrically with said circuit elements;

a step of forming, at the stage for forming said multilayer wiring part, a plurality of holes toward a second main surface to become an opposite face against said first main surface of said semiconductor substrate from specified depth of said multilayer wiring part having an insulating film on their surfaces and of forming filling electrodes to fill those holes

with conductive substance and be electrically connected with specified wiring of said multilayer wiring part;

a step of forming a first insulating layer on the first main surface of said semiconductor substrate;

a step of removing the second main surface of said semiconductor substrate from its surface by specified thickness to expose said filling electrodes to form through-type electrodes;

a step of removing by etching the second main surface of said semiconductor substrate by specified thickness to cause said through-type electrodes to protrude by specified length;

a step of forming a second insulating layer of specified thickness on the second main surface of said semiconductor substrate in a state of exposing forward ends of said through-type electrodes;

a step of forming protruding electrodes at exposed portions of said through-type electrodes; and

a step of cutting said semiconductor substrate inclusive of said first and second insulating layers in a lattice pattern to divide said respective product forming parts.

26. The process for fabricating a stacked semiconductor device according to claim 24, characterized in that said second semiconductor device having only said post electrodes is formed through:

a step of aligning, disposing and forming a plurality of product forming parts inclusive of specified circuit elements on a first main surface of a semiconductor substrate;

a step of forming a multilayer wiring part in said respective product forming parts by laminating and forming sequentially in a specified pattern wiring and insulating layers being connected electrically with said circuit elements;

a step of forming post electrodes on respectively specified wiring of said multilayer wiring part;

a step of forming, on the first main surface of said semiconductor substrate, a first insulating layer to cover said post electrodes;

a step of removing the surface of said first insulating layer by specified thickness to expose said post electrodes;

a step of removing the second main surface of said semiconductor substrate from its surface by specified thickness to make said semiconductor substrate thin;

a step of forming a second insulating layer of specified thickness on the second main surface of said semiconductor substrate;

a step of forming protruding electrodes at exposed portions of said post electrodes; and

a step of cutting said semiconductor substrate inclusive of said first and second insulating layers in a lattice pattern to divide said respective product forming parts.

27. The process for fabricating a stacked semiconductor device according to claim 24, characterized by:

having a step of stacking and securing one to a plurality of third semiconductor device (devices) stacked and secured

between said first semiconductor device and said second semiconductor device through said step (a) to step (k);

forming filling electrodes provided on one surface of said third semiconductor device so as to correspond with the filling electrodes or the post electrodes of the facing semiconductor device; and

forming post electrodes provided on the other surface of said third semiconductor device so as to correspond with the filling electrodes or the post electrodes of the facing semiconductor device.

28. The process for fabricating a stacked semiconductor device according to claim 24, characterized in that a plurality of second semiconductor devices smaller than said first semiconductor device are disposed and secured in parallel on said first semiconductor device.

29. The process for fabricating a stacked semiconductor device according to claim 24, characterized in that the respective filling electrodes or respective post electrodes on the upper surface of said first semiconductor device are formed so as to correspond with the respective filling electrodes or respective post electrodes on the lower surface of said second semiconductor device.

30. The process for fabricating a stacked semiconductor device according to claim 24, characterized in that:

in said step (e), at the time of forming said first insulating layer, resin hardening processing is set to insufficient primary hardening processing;

in said step (f), after exposing said post electrodes on the surface of said first insulating layer, secondary hardening processing accompanying hardening contraction of said first insulating layer is implemented to expose forward ends of said post electrodes on the surface of said first insulating layer;

at the time when said second semiconductor device is stacked and secured onto said first semiconductor device, ultrasonic oscillation is applied to the protruding portions of said post electrodes to be brought into connection with facing said filling electrodes or said post electrodes by metal joint.

31. The process for fabricating a stacked semiconductor device according to claim 24, characterized by forming said post electrodes with a plating film, stud bump electrodes or a CVD film.

32. The process for fabricating a stacked semiconductor device according to claim 24, characterized by:

interposing a metal plate having insulating holes between said first semiconductor device and said second semiconductor device,

in the portion of said insulating holes, electrically connecting said filling electrodes or said post electrodes on the upper surface of said first semiconductor device with said filling electrodes or said post electrodes on the lower surface of said second semiconductor device with temporary melting treatment applied to said protruding electrodes, and electrically connecting said through-type electrodes and said

post electrodes of the first semiconductor device and said second semiconductor device to face said metal plate with said metal plate with temporary melting treatment applied to said protruding electrodes.

33. The process for fabricating a stacked semiconductor device according to claim 32, characterized by connecting said filling electrodes or said post electrodes to be given power supply potential of said semiconductor device or ground potential with said metal plate.

34. The process for fabricating a stacked semiconductor device according to claim 24, characterized by filling a gap between said first semiconductor device and said second semiconductor device with insulating resin to harden it.

35. The process for fabricating a stacked semiconductor device according to claim 24, characterized by using a silicon substrate as said semiconductor substrate for one semiconductor device out of said first and second semiconductor devices to form said circuit elements and using a compound semiconductor substrate as said semiconductor substrate for the other semiconductor device to form said circuit elements.

36. The process for fabricating a stacked semiconductor device according to claim 24, characterized by, in fabricating said second semiconductor device, likewise said first semiconductor device, forming a plurality of post electrodes exposed in a surface of said first insulating layer and a plurality of through-type electrodes exposed in a surface of said second insulating layer, and providing protruding

electrodes to exposed ends of specified said post electrodes or said through-type electrodes to become the upper surface.

37. The process for fabricating a stacked semiconductor device according to claim 24, characterized by forming said post electrodes larger than said through-type electrodes in diameter.

38. The process for fabricating a stacked semiconductor device according to claim 24, characterized by forming active elements and passive elements as said circuit elements.

39. The process for fabricating a stacked semiconductor device according to claim 24, characterized by

in said step (e), forming said first insulating layer to have thickness of around 20 to 100 μm;

in said step (c), forming said holes to have depth of around 5 to 50 μm;

in said step (f), forming said post electrodes to have thickness of around 20 to 100 μm; and

in said step (g), forming said through-type electrodes to have thickness of around 5 to 50 μm.

40. A process for fabricating a semiconductor device, characterized by having:

(a) a step of aligning, disposing and forming a plurality of product forming parts inclusive of specified circuit elements on a first main surface of a semiconductor substrate;

(b) a step of forming a multilayer wiring part in said respective produce forming parts by laminating and forming sequentially in a specified pattern wiring and insulating

layers being connected electrically with said circuit elements;

(c) a step of forming, at the stage for forming said multilayer wiring part, a plurality of holes toward a second main surface to become an opposite face against said first main surface of said semiconductor substrate from specified depth of said multilayer wiring part having an insulating film on their surfaces and of forming filling electrodes to fill those holes with conductive substance and be electrically connected with specified wiring of said multilayer wiring part;

(d) a step of forming post electrodes on respectively specified wiring of said multilayer wiring part;

(e) a step of forming, on the first main surface of said semiconductor substrate, a first insulating layer to cover said post electrodes;

(f) a step of removing the surface of said first insulating layer by specified thickness to expose said post electrodes;

(g) a step of removing the second main surface of said semiconductor substrate from its surface by specified thickness to expose said filling electrodes to form through-type electrodes;

(h) a step of removing by etching the second main surface of said semiconductor substrate by specified thickness to cause said through-type electrodes to protrude by specified length;

(i) a step of forming a second insulating layer of specified thickness on the second main surface of said

semiconductor substrate to expose forward ends of said through-type electrodes; and

(j) a step of cutting the said semiconductor substrate inclusive of said first and second insulating layers in a lattice pattern to divide said respective product forming parts.

41. The process for fabricating a semiconductor device according to claim 40, characterized in that:

in said step (e), at the time of forming said first insulating layer, resin hardening processing is set to insufficient primary hardening processing; and

in said step (f), after exposing said post electrodes on the surface of said first insulating layer, secondary hardening processing accompanying hardening contraction of said first insulating layer is implemented to expose forward ends of said post electrodes on the surface of said first insulating layer.

42. The process for fabricating a semiconductor device according to claim 40, characterized by forming protruding electrodes at specified exposed portions of said through-type electrodes and said post electrodes after said step (i) or after said step (j).

43. The process for fabricating a semiconductor device according to claim 40, characterized by forming said post electrodes larger than said through-type electrodes in diameter.

44. The process for fabricating a semiconductor device according to claim 40, characterized by forming said post

electrodes with a plating film, stud bump electrodes or a CVD film.

45. The process for fabricating a semiconductor device according to claim 40, characterized in that said circuit elements are active elements and passive elements.

46. The process for fabricating a semiconductor device according to claim 40, characterized by

in said step (e), forming said first insulating layer to have thickness of around 20 to 100 μm;

in said step (c), forming said holes to have depth of around 5 to 50 μm;

in said step (f), forming said post electrodes to have thickness of around 20 to 100 μm; and

in said step (g), forming said through-type electrodes to have thickness of around 5 to 50 μm.